High fidelity digital front-end system for digital radio measurement in the DRM band

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Abstract- This document describes the design and implementation of a high fidelity instrumentation digital radio front-end, following the standard DRM “Digital Radio Mondiale” [1]. This approach meets the need of measurement equipment in the planning steps preceding digital radio commercial operation.

The front-end captures AM band signal from an antenna, filters and digitalizes a specified frequency channel by means of undersampling techniques, and transmits its samples in real time through an Ethernet network towards a computer, namely back-end, which is responsible for demodulation. The design is intended to minimize hardware process as far as possible, in order to provide flexibility and minimize distortion. Procedures for remote configuration and status feedback of the front-end are specified as well.

I. INTRODUCTION AND MOTIVATION

The progressive digitalization of communication systems, with inherent benefits in terms of flexibility and reliability, has led to the specification of the DRM standard (Digital Radio Mondiale), which is applicable to the AM broadcasting band, from 0 to 30 MHz. Within the analysis and planning of new networks it is necessary to develop instrumentation equipment that allows measurement of signal reception quality in different geographical locations, in order to corroborate theoretical propagation models.

This project is part of a TSR Group’s research line, with the aim to design and implement a complete digital instrumentation DRM receiver.

II. GENERAL DESCRIPTION OF THE SYSTEM

![Fig. 1. Block diagram of the receiver.](image)

The receiver’s high level architecture is shown in Fig. 1. Two main subsystems are defined: a front-end (A, B, C) which obtains the samples of a selected channel within the DRM band from an antenna input; and a personal computer, namely back-end, with a software responsible for signal demodulation and source decoding (E). These subsystems are interconnected by means of an Ethernet local area network (D). The development of the back-end’s software is out of the scope of this document.

The front-end consists of three functional blocks: an analog processing module (A); a communications module (C) with a commercial Ethernet controller CI (C); and a development kit with two Digital Signal Processors (DSPs) (B) (ADSP TS101S Ez-Kit Lite from Analog Devices), one to be used for digital processing and the other one implementing a control unit.

III. TECHNICAL CHARACTERISTICS

The front-end must satisfy the following technical specifications regarding to its input and output signals:

- Digitalization of any channel with a 20 kHz bandwidth within the DRM (AM) band.
- Transmission of the digitalized samples over an Ethernet network with a sampling rate of 48 ksamples/s, using UDP as transport protocol and 100 samples per frame.

IV. SIGNAL TREATMENT DESCRIPTION

A. Theoretical fundamentals

The front-end is designed in the digital domain as far as possible so as to reduce analog distortion, noise and drifts which result in degradation of measurement quality.

Nyquist criterion states that \( f_s \geq 2 \cdot \text{BW} \), where \( f_s \) is the sampling frequency of a digitalized analog signal and \( \text{BW} \) is its bandwidth.

A digitalization of all DRM band with its subsequent digital processing requires excessive digital processing capacities for the state-of-the-art commercial DSPs, due to the need to deal work with a sampling rate of 2-30 MHz = 60 Msamples/s in real time. However, in the case of the described design, only a narrow band portion (20 kHz) of the DRM band is captured. Therefore it is possible to use a lower sampling frequency, \( f_s' \). After the digitalization, all spectral components of the subbands \([0, f_s'/2], [f_s'/2, f_s'], \ldots, [4f_s'/2, (i+1)f_s'/2] \) are translated to the subband \([0, f_s'/2] \). (\( i \) from 0
to \( \pi \) in the digital domain). If one subband is band-pass filtered and afterwards it is digitized with a sampling frequency \( f'_s \), the observed effect is the same as a frequency down conversion followed by digitalization. Thus it is possible to reduce the sample rate to be processed by the DSPs. This technique is known as undersampling [2].

B. Analog processing

**HIGH LEVEL DESIGN**

As it is shown in Fig. 2., the system input is an analog signal captured by an antenna \( s_a(t) \). After a preconditioning stage (variable attenuator), a desired bandwidth of the DRM band is selected using an analog filter bank and a DSP controlled switch (see figure C2). The obtained analog signal \( x_a(t) \) is digitized by means of an analog to digital converted (ADC), previously adjusting its gain with an automatic gain control system (AGC), which interfaces to a variable gain amplifier (VGA). This amplifier is located after the filter bank so as to avoid crosstalk interference between channels. A more selective filtering is achieved in the digital domain.

![Fig. 2. Analog processing](image)

**COMMUNICATION BETWEEN ADC AND DSPs**

The communication between ADC and DSPs is implemented with an asynchronous architecture, using a FIFO memory (First In, First Out), as shown in Fig. 3.

In order to avoid processor cycle consumption in the acquisition of digitalized samples, a DMA (Direct Memory Access) module included in the DSPs is used. The sample treatment is done in blocks, each of which gives an output of 100 samples that are encapsulated within an Ethernet frame. The data transfers, considering that the output sampling rate is 48 ksamples/s, and that the input sampling rate is 60 Msamples/s, must satisfy the following condition:

\[
N_{\text{samples/block}} = \frac{60\text{Msamples/s}}{48\text{ksamples/s}} = n \times 1250, n \geq Z \quad (1)
\]

Two memory buffers are defined within the FIFO memory, so as not to overwrite the first buffer’s data as it is transferred to the DSPs. An adequate FIFO size is 8Kx16bits.

In the software’s flux diagram two interrupts are relevant: **INT FIFO**, which informs the DSP of a partial FIFO memory load (half of its capacity), and leads to the beginning of a DMA transfer; and **INT DMA**, which shows that there is a sample block to be processed.

![Fig. 3. Communication between ADC and DSPs](image)

**ANALOG FILTERING DESIGN**

The most relevant problem in an undersampling design is the achievement of feasible analog filtering specifications with a reduced number of electronic components. Transition bands in the filtering characteristics appear, (see Fig. 4.), which should be centred in only one of the \([fS/2, (i+1)fS/2]\) subbands, if aliasing effects are to be prevented. Thus there are frequency ranges around \(fS/2\) in which information capture is not directly possible.

![Fig. 4. Analog filtering frequency specifications](image)

An approach to this problem is to introduce a series of “secondary” filters with passbands which correspond to the transition bands of the “main” filters. This method allows capturing signal in all the DRM band. These additional analog filters must be centred on a \([fS/2, (i+1)fS/2]\) subband, therefore avoiding aliasing distortion in the digitalization process. Note that aliasing is allowed in the transition bands of the filters since no signal will be captured in these.

The only feasible mathematical solution for this design model is to introduce several sampling frequencies, one of which will be selected depending on which analog filter is used to extract the desired channel information. Different decimation factors \( (N_i) \) are introduced in the samples stored by the DMA by simply reading non-consecutively the
memory map of the DSPs. The true sampling frequency is computed as follows:

\[ f_s' = \frac{f_s}{N_i} \]

The required processing capacity is given by the \( N_i \) which corresponds to the “main” analog filters. For the commercial processors which have been used in the implementation, a value of \( N_i = 8 \), which implies a sampling rate of \( f_s' = 7.5 \text{ Msamples/s} \), is enough. Therefore \( 15 \text{ analog filters} \) are needed.

The decimation values corresponding to the “secondary” analog filters must result into passband frequency ranges fitting to the desired filtered subbands, being also integer divisors of the sampling frequency of the ADC, so as to simplify the digital processing chains. A sampling frequency of \( f_s = 60 \text{ Msamples/s} \) is adequate, since there are enough values of \( N_i \) (8, 10, 12, 15) to undertake the implementation.

Passive components (\( L, C \)) are used to design the analog filters, so as to minimize non-linear effects, following a minimum number of electronic components criterion. Design parameters are shown in Fig. 5. SMD components (Surface Mounting Devices) are used, with parallel and serial configurations to compensate for component tolerance

<table>
<thead>
<tr>
<th>Filter type</th>
<th>Structure</th>
<th>Number of components</th>
<th>Range of capacitive and inductive values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-pass</td>
<td>Cauer (Order 5)</td>
<td>7</td>
<td>( L_{\text{min}}=6.295 \text{ nH} ) ( L_{\text{min}}=6.780 \text{ uH} ) ( C_{\text{min}}=6.77 \text{ pF} ) ( C_{\text{min}}=7.297 \text{ nF} )</td>
</tr>
<tr>
<td>Band-pass</td>
<td>Cauer (Order 3)</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Passband ripple ( &gt;=1.5 \text{ dB} ) Stopband isolation ( &gt;=30 \text{ dB} )</td>
<td></td>
</tr>
</tbody>
</table>

**Fig. 5. Analog filters characteristics**

**OTHER ANALOG PROCESSING FEATURES**

Two relay banks are used for analog filters selection (see Fig. 6); both at input and output, in order to minimize signal attenuation (which would lead to a higher noise level in the receiver) and distortion and so as to achieve a good isolation which prevents crosstalk interference. The switching architecture is controlled by the DSPs using a serial line and a Serial to Parallel Converter.

**Fig. 6. Analog switching.**

A commercial variable attenuator and AGV will be used with a similar interfacing method from the DSP architecture.

**C. Digital processing**

Fig. 7 shows the different digital processing stages: first a decimation process, in order to achieve a reduced sampling frequency \( f_s' \); then a multiplication by a complex tone with the 20kHz bandwidth channel’s central frequency \( f_c \), so as to translate it to baseband \( f_c \); a low-pass filtering and decimation \( (N_i) \) chain, in order to achieve a 48 kHz sampling rate with the desired channel’s information. In some situations sample interpolation will be required, though this should be prevented as far as possible so as to reduce processing load, which allows using the free processor cycles to improve the digital filters selectivity.

**Fig. 7. Digital processing**

Butterworth IIR filters are used, with \( i \)-2 orders \( (i: \text{ digital filtering stage index}) \). Pipelining (multiprocess) techniques are used for a feasible implementation, therefore achieving important reductions in required processor cycles per sample. Moreover decimation and filtering are implemented at one single stage, computing only the samples which are necessary for subsequent stages after decimation. For instance, in the case of an order 2 filter:

\[ y[n] = w[n] + b_1 \cdot w[n-1] + b_2 \cdot w[n-2] \]
\[ w[n] = g \cdot x[n] + a_1 \cdot w[n-1] + a_2 \cdot w[n-2] \]

If a decimation stage follows the filtering it will only be necessary to compute both \( y[n] \) and \( w[n] \) for the samples that will be kept after decimation, and \( w[n] \) for the rest of them.

There are required as many processing chains as different sampling frequencies \( f_s' \) are in the system. Furthermore in \([i \cdot f_s'/2, (i+1) \cdot f_s'/2] \) subbands, ‘i’ being an even figure, an undersampling process produces a spectral rotation which can be reverted by:

- Processing the real samples at the beginning of the chain:
  \[ y[n] = (-1)^i \cdot x[n] \]  \hspace{1cm} (4)
- Processing the complex samples at the end of the chain:
  \[ y[n] = \text{Re}\{x[n]\} - \text{Im}\{x[n]\} \]  \hspace{1cm} (5)

It follows that it is enough to change the last processing stage in accordance with the selected analog filter.
OTHER DIGITAL PROCESSING FEATURES

A digital automatic gain control (AGC) is implemented. This approach is based on the calculation with a slow rate of the overflows proportion in a block of processed samples, as well as the number of samples with zero-valued most significant bit. If some defined thresholds are exceeded, in the first case the gain of the AGV shall be reduced or the attenuation be increased. In the second case an opposite procedure will be followed.

V. ETHERNET COMMUNICATIONS MODULE DESCRIPTION

A. Hardware architecture

Fig. 9 shows the implemented hardware architecture. A commercial Ethernet controller CI is used (SMSC LAN91111) to implement IEEE 802.3 PHY and MAC layers. Its access interface consists of a group of memory mapped registers through which the controller is configured, its status is read, or data frames are transmitted or received. Furthermore the controller includes an interrupt line (INT Ethernet) to provide asynchronous status information (link failure, frame transmitted or received successfully, etc.). The output interface consists of a RJ45 connector to be interfaced by an Ethernet switching device.

One of the DSPs is able to access the samples processed by the other one, and it is informed of data availability by means of an interrupt (INT DSPA)

\[ \text{INT DSPA} \rightarrow \text{INT Ethernet} \]

\[ \text{DATA} \]

\[ \text{DSP A} \rightarrow \text{DSP B} \rightarrow \text{MAC/PHY} \rightarrow \text{RTCP} \rightarrow \text{LAN} \]

Fig. 9. Communications hardware architecture

B. Protocol logic architecture

Fig. 10. and Fig. 11. show the communication protocols which are implemented over Ethernet’s MAC level. A user plane is defined to describe the unidirectional transmission of data from the front-end to the back-end over RTP (Real Time Protocol) [3]; as well as a control plane which is responsible for telemetry and telecommand procedures from the back-end executed remotely in the front-end with a bidirectional simplex architecture (no new requests are admitted in the back-end before a confirmation of the latest is achieved). The control plane is implemented over RTCP (Real Time Control Protocol) and DCP (Distribution & Communication Protocol) [4].

\[ \text{User plane} \rightarrow \text{Control plane} \]

\[ \text{DRM Data} \rightarrow \text{DRM profile} \]

\[ \text{RTP} \rightarrow \text{DCP Tag Layer} \rightarrow \text{RTCP} \]

\[ \text{UDP} \rightarrow \text{ARP} \]

\[ \text{IP v.4} \rightarrow \text{Ethernet MAC/PHY} \]

\[ \text{ICMP} \rightarrow \text{IP v.4} \rightarrow \text{Ethernet MAC/PHY} \]

Fig. 10. Protocol architecture

Message Type Function
red \text{c, m, r} \quad \text{Reading or configuration of IP and MAC addresses, RTP/RTCP ports,} \text{etc.}
inf \text{g, r} \quad \text{General information about front-end (manufacturer, model identifying data, ...)}
rst \text{c, r} \quad \text{Resets the front-end.}
txd \text{g, c, r} \quad \text{Starts or stops sample transmission.}
tx \text{g, c, m, r} \quad \text{Tunes a frequency channel.}
aln \text{g, c, m, r} \quad \text{Adjust AGV’s gain manually.}
alt \text{g, c, m, r} \quad \text{Adjust front-end’s attenuation manually.}
sou \text{g, c, m, r} \quad \text{Chooses input impedance (600 Ω or 50 Ω).}
cag \text{g, c, m, r} \quad \text{Activates or deactivates CAG.}
drm \text{g, c, m, r} \quad \text{Encapsulates of messages in one frame.}

Fig. 11. Protocol procedures and telecommand and telemetry messages.

VI. CONCLUSIONS

A digital front-end with analog processing using undersampling techniques provides a way to eliminate the non-linear signal distortion introduced by the traditional analog mixers, at the expense of introducing a high number of filtering passive components. An Ethernet communication is adequate for this receiver architecture: with enough data transmission capacity, it allows flexibility and is compatible with a computer’s typical network interfaces.

The next challenge is to combine undersampling and digital processing with DSPs and FPGAs in order to capture signal from the DRM+ band (up to 150MHz).

VII. ACKNOWLEDGEMENT

The authors acknowledge the collaboration of Signal Treatment and Radiocommunications Group (TSR) members in the development of the described project and in the writing of this document.

VIII. REFERENCES